High resolution, steep profile resist patterns

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High resolution and steep profile patterns have been generated in a 2.6 μm thick organic layer which conforms to the steps on a wafer surface and is planar on its top. This thick organic layer (a photoresist in the present experiments) is covered with an intermediate layer of SiO_2 and a top, thin layer of x-ray or photoresist. After exposure and development of the top resist layer, the intermediate layer is etched by CHF_3 reactive ion etching. The thick organic layer is then etched by O_2 reactive ion etching. Submicron resolution with essentially vertical walls in the thick organic material was achieved. The technique is also applicable to photo and electron lithography. It reduces the need for thick resist patterns for the lithography step and, at the same time, ensures high resolution combined with good step coverage.

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I. INTRODUCTION

With the advent of higher resolution lithographies, such as x ray[1,2] and electron beam, as well as increased resolution from optical lithography, there is a demand for using these capabilities for making VLSI devices. Often, the ability to achieve good linewidth control, high resolution, and good step coverage tend to be mutually exclusive. Good step coverage requires thick resist while high resolution is more easily obtained in thin resist.[3] This is true for all resists, both positive and negative.

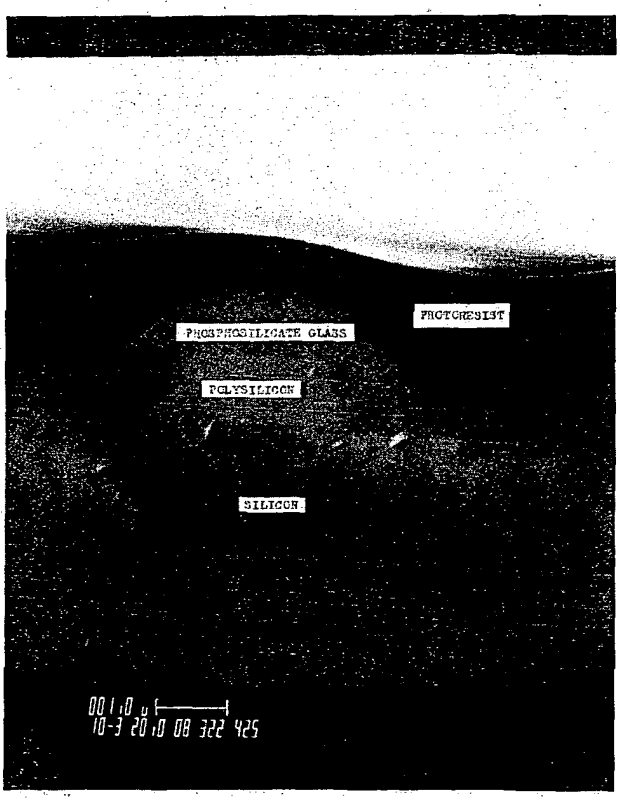

FIG. 1. X-ray resist thickness variation as it step covers 1.0 μm of p-glass flowed over a 1.0 μm high poly-silicon feature. Resist varies from 0.8 μm on top of the feature to 1.7 μm in the valley between features (SEM profile photo).

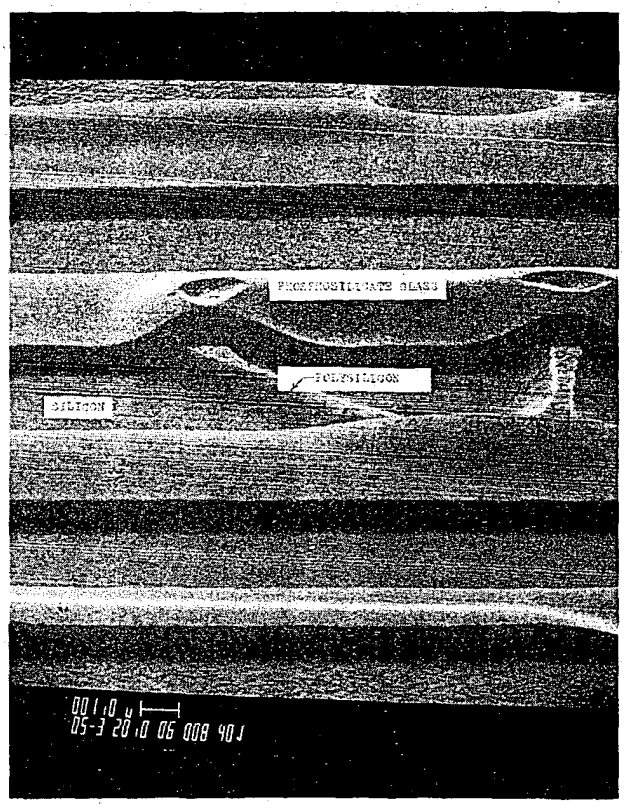

FIG. 2. Result of plasma etching p-glass when the resist is too thin on top of the feature. The holes in the p-glass (the resist has been stripped away) indicate resist erosion on top of the feature. (SEM photo).

With any resist, the ideal conditions for obtaining high resolution and good linewidth control are a flat surface and a thin resist (0.3–0.4 μm). The flat surface ensures that the spun-on resist has very little variation in thickness and, as a result, there should be little variation in resist linewidth. However, resist linewidth variations will occur when lines traverse a step. Figure 1 illustrates the variation in resist

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thickness, of the spun-on resist, as it covers a 1.0 μm thick phosphosilicate glass flowed over a 1.0 μm thick polysilicon step. The darker area is the resist which measures 0.8 μm thick on top of the feature and 1.7 μm thick in the valley between features.

Patterning a wafer with resist thickness variations as shown in Fig. 1 will result in both a difference in feature size as well as a very thin resist on top of the step. In the case of a chemical etch, the thin resist does not present a problem. However, if plasma etching is used, the resist is relied on as a mask. For a thin resist, the result of plasma etching the phosphosilicate glass is shown in Fig. 2. The horizontal lines are p-glass which has been etched. The slant line and vertical line in the center of the photo are polysilicon steps. Note that there are two round holes in the p-glass where it goes over the step. This is due to erosion of the thin resist on the step during plasma etching of the p-glass. The resist has been stripped completely away to reveal this problem.

Presented here is a method for generating high resolution, steep profile resist patterns by first preparing a flatter surface on the wafer. This is done by spinning a thick organic layer of resist which conforms with the wafer surface and is planar on its top. Figure 3 illustrates this with a 2.6 μm thick layer of HPR-206 spun down on the same topography shown in Fig. 1. The curved, lighter area is the p-glass and the rough darker area on top is the thick resist. The thick layer is then patterned using an intermediate masking layer of plasma deposited SiO_2 and a thin top layer of resist. The result is that a very thick resist material can be patterned with submicron resolution and steep sidewalls comparable with those in positive photoresist.

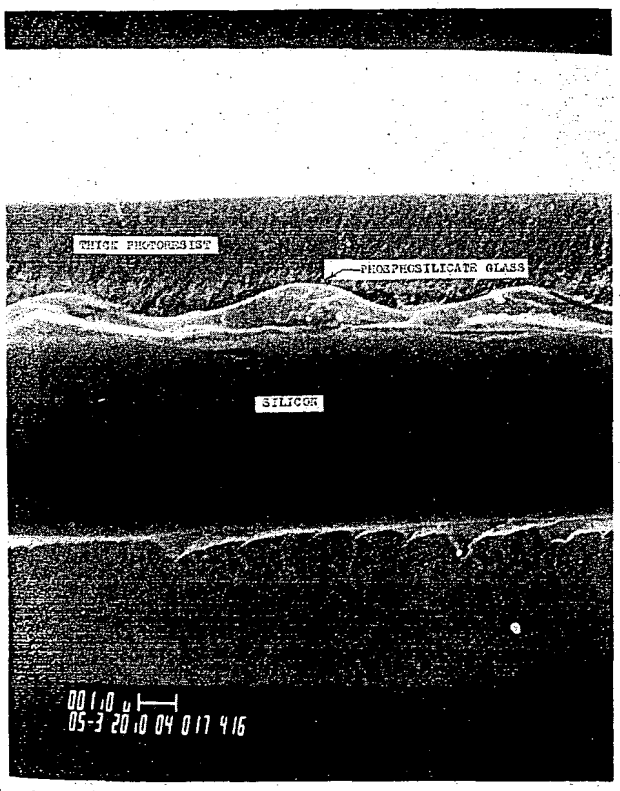


FIG. 3. SEM profile of a very thick resist covering the same features as shown in Fig. 1. Note the flat surface due to the very thick resist spun-on the surface.

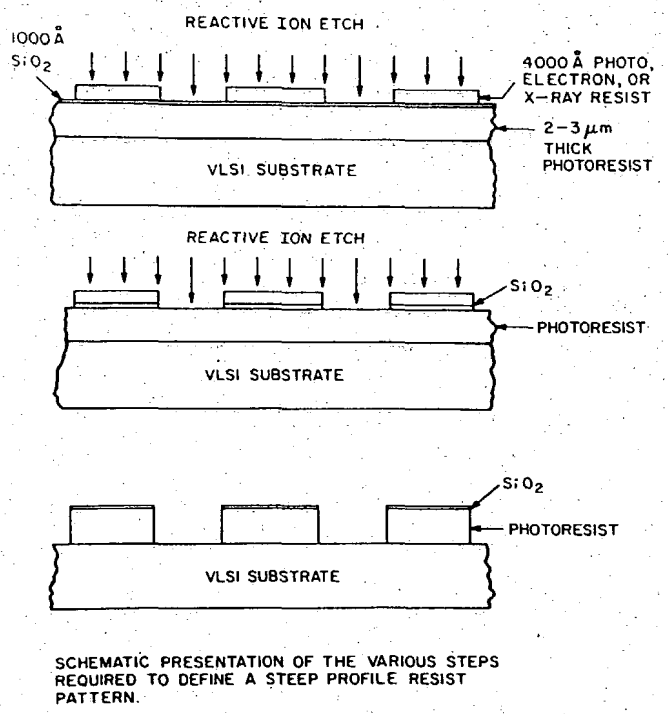


FIG. 4. Processing sequence for three level, high resolution patterning.

II. EXPERIMENT

A 2.6 μm thick layer of photoresist (HPR-204-Hunt Chemical Co.) serving as the thick organic layer, was spun on a silicon wafer. The intermediate layer of 0.10 μm of silicon

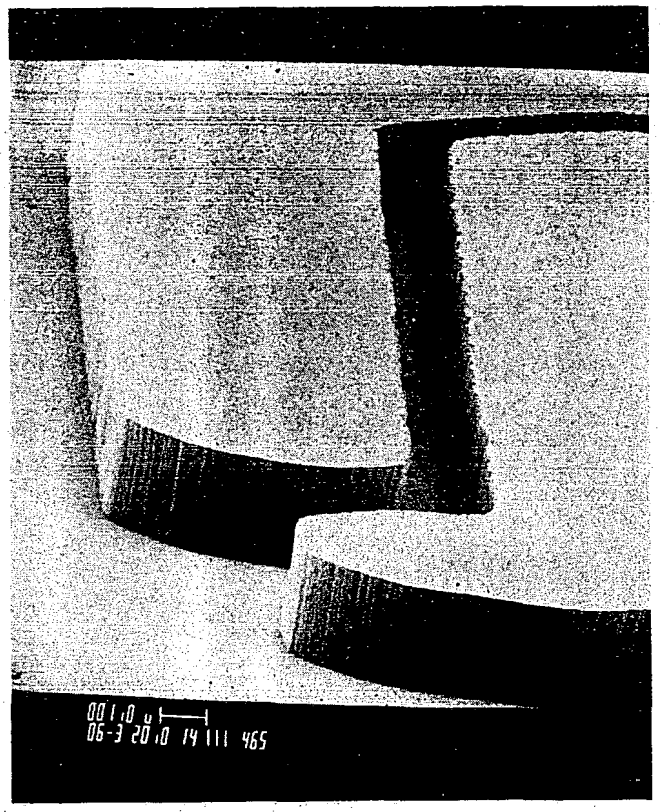


FIG. 5. Resulting pattern, which is all thick HPR resist, after using the trilevel processing described in Fig. 4. Top pattern was done with x-ray resist. The walls are 90° and there is no linewidth loss (SEM photo).

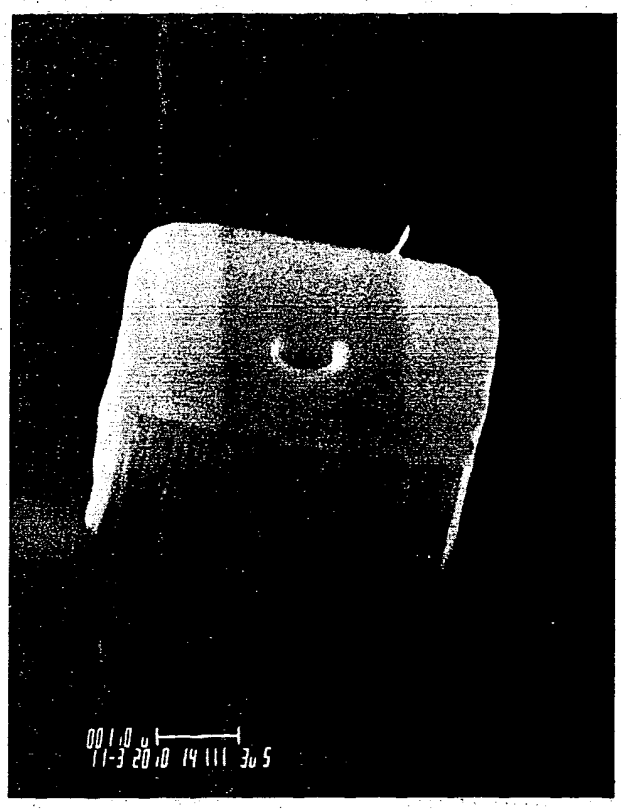


FIG. 6. A submicron window, in 2.1 μm thick resist using the trilevel technique and x-ray patterning (SEM photo).

TABLE I. High resolution, steep profile resist patterns.

Advantages
1. Planar surface for resist patterning
2. Excellent step coverage
3. Good linewidth control
4. Thinner resist can be used for better resolution
5. Eliminates standing waves and scattering in photolithography
6. Reduces proximity effects in electron lithography
7. Minimal resist erosion during substrate etch by plasma or ions
Disadvantages
1. Requires extra processing steps

dioxide was plasma deposited, at 200°C, on the photoresist and then a 1.0 μm thick layer of chlorine based negative x-ray resist[4] was deposited on top of the oxide. A schematic presentation of the processing sequence is shown in Fig. 4.

The top layer of x-ray resist was exposed and developed to a final thickness of 0.45 μm using an x-ray exposure tool.[1,2] With the x-ray resist as a mask, the SiO_2 was reactive ion etched with a CHF_3 gas. The pattern was then transferred into the thick organic (resist) layer using reactive ion etching, with pure O_2 gas forming the plasma and the SiO_2 acting as the mask. The rf power density was 0.30 W/cm^2 and the time required to etch the resist was 20 min. Figure 5 shows the resultant pattern which is 2.6 μm high and has a trench width of 1.5 μm. The photos are taken with a scanning electron microscope at a very steep angle so as to clearly show the wall structure of the resist. Note that the walls are perpendicular

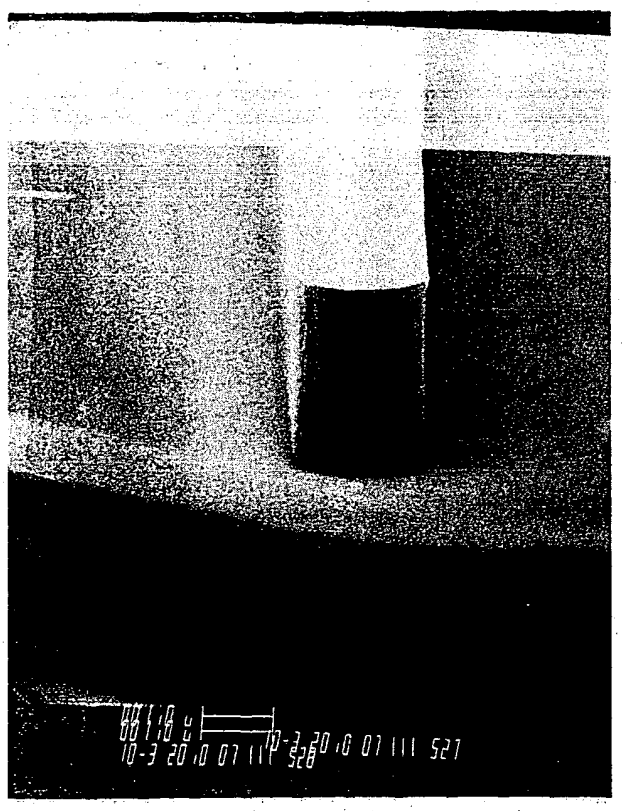


FIG. 7. Thick resist pattern obtained using optical patterning on a Perkin–Elmer projection printer for the top layer. (SEM photo).

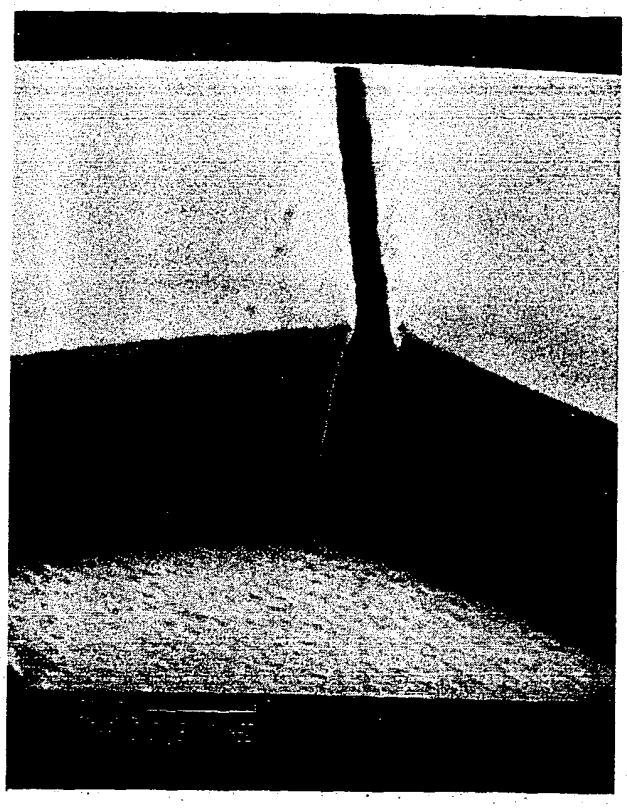


FIG. 8. Submicron trench for a Ga As gate obtained using a Kasper 10:1 step and repeat camera for the top layer. (SEM photo).

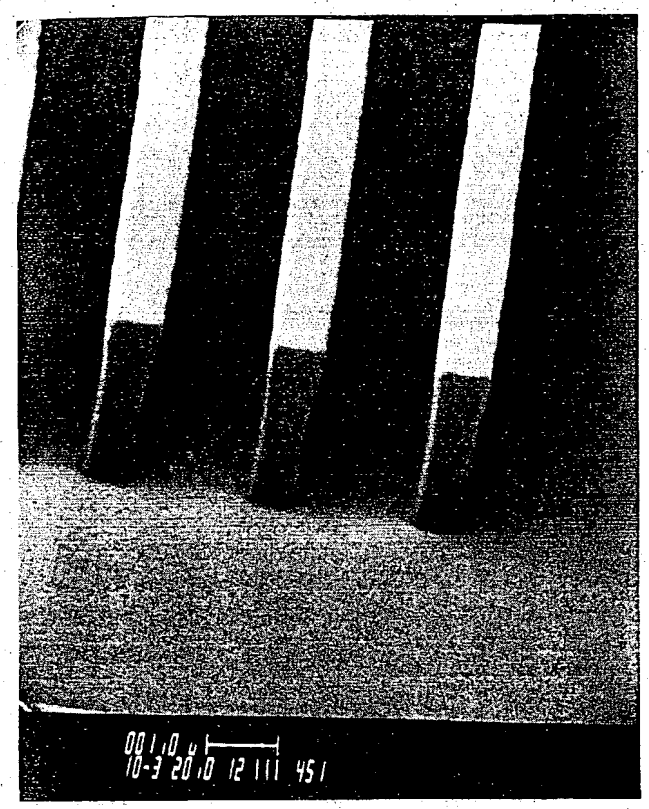
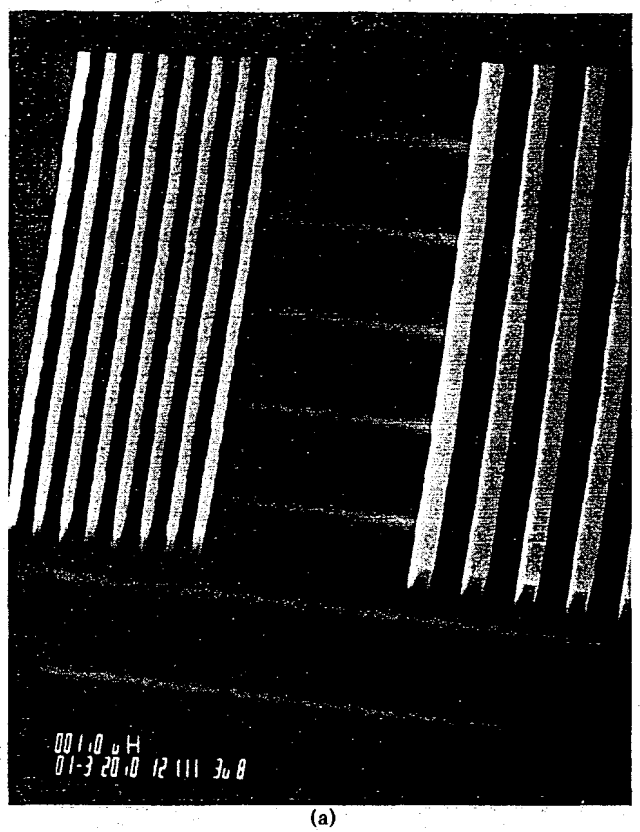
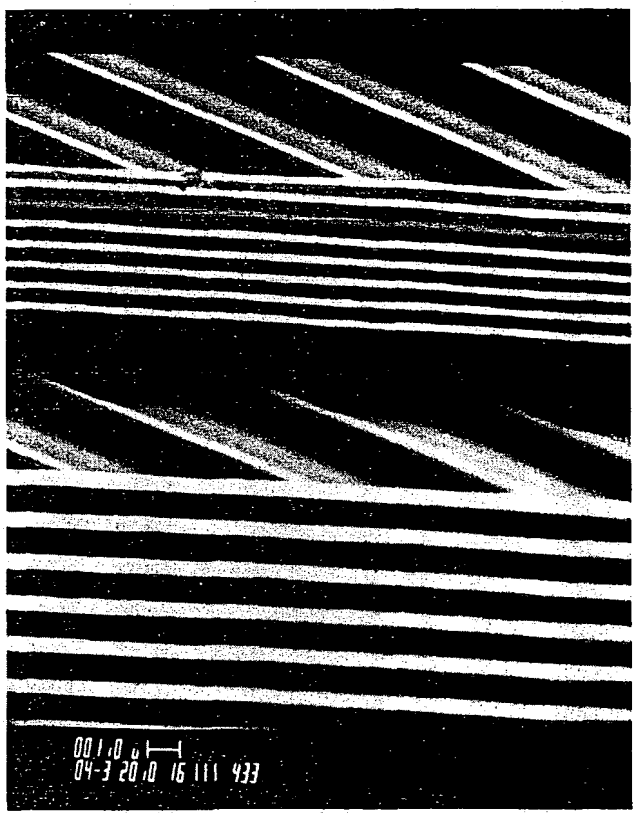


FIG. 9. Lines and spaces obtained using the trilevel technique with a negative electron resist (GMC) for the top patterning layer (SEM photo).



(a)



(b)

FIG. 10. (a) 1.0 μm lines and spaces in thick resist, using x ray for the top layer. The lines are traversing a 1.0 μm high, periodic grating to demonstrate good step coverage with no linewidth variation over steps (SEM photo). (b) Profile of the wall of resist for one of the 1.0 μm lines showing conformal coating of the wafer topology at the resist bottom and a flat surface at its top (SEM photo).

and there is very little undercut. The oxide is still on top of the organic (resist) layer and its thickness loss during the reactive ion etch was less than 0.02 μm. Table I lists the advantages and disadvantages of this technique herein denoted as the tri-level technique.

Figure 6 is an SEM photograph of the high resolution capability of the combination of the tri-level structure and a high resolution x-ray resist.[4] A 0.5 μm window has been transferred to a 2.1 μm thick photoresist layer with no perceptable undercut apparent.

II. DISCUSSION

The tri-level technique for obtaining high resolution features in thick resist can be applied to other lithographies besides x-ray lithography since there are advantages for optical and electron-beam lithography as well.

In the case of optical lithography; the thick underlying layer of resist and the intermediate layer of SiO_2 significantly reduce reflection from the wafer surface and, as a result, reduce standing wave problems. The flat surface of the thick organic layer keeps scattering down and the top resist can be made thin for high resolution. There is also the advantage of having the same surface to coat and expose on for all process levels which means a fixed exposure time, developing time, and a consistent surface for the top resist to be coated on every time. Figures 7 and 8 are SEM photos of results obtained from an optically exposed top resist layer. Figure 7 is a 2.0 μm wide feature, 2.6 μm high, that is routinely achieved on a device wafer using a Perkin–Elmer projection printer and HPR-204

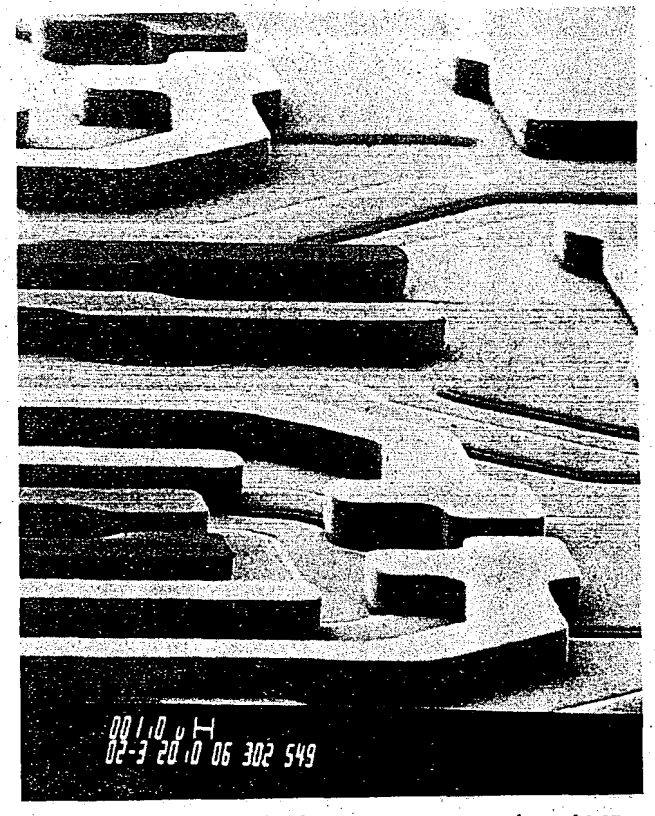


FIG. 11. Application of the trilevel resist to reactive ion etching of 0.65 μm of polysilicon on a device wafer. The thick resist is still on and is used as the etch mask.

photoresist. The thin 0.1 μm thick SiO_2 layer can just be seen at the top of the feature. Figure 8 is a submicron trench that was patterned using a Kasper 10:1 step and repeat camera.

For electron-beam lithography, backscattering from a substrate covered by 0.1 μm of SiO_2 on top of 2.6 μm of polymer is less than that from an Si or SiO_2/Si substrate because of the lower atomic number material. Thus, proximity effects for thick resists (>0.5 μm) are reduced and better linewidth control has been observed with both negative and positive resists. In addition, high speed electron resists, such as GMC[5] or PBS,[6,7] can be used for patterning of wafers since the top layer of resist need not be thick. Figure 9 shows an SEM photo of a tri-level pattern in which 0.5 μm thick GMC was used to generate the initial pattern. The lines are 0.75 μm wide and the space is 1.5 μm.

In the case of x-ray lithography, the resist currently being used for direct wafer exposure is a negative, high speed resist. However, 1 μm resolution is only possible[4] when the final resist thickness is $\leq$0.4 μm. This precludes using it for direct wafer exposure since it does not have good plasma resistance. However, the tri-level technique permits the use of thin resists, since there are no steps. Figure 10(a) shows an SEM photo of both 1 μm and 2 μm lines and spaces traversing a 1 μm high p-glass step. The light lines running vertically are the final tri-level resist lines initially patterned with a 0.45 μm of x-ray resist. The horizontal lines are the p-glass-covered 1 μm high polysilicon steps. Figure 10(b) is also an SEM photo, at a very shallow angle, of the broadside of the 1 μm lines and spaces demonstrating the flatness of the top surface and the conformal coating of the step.

Finally, we would like to indicate the usefulness of this technique for patterning device wafers. This technique has been used for patterning silicon nitride, polysilicon, phosphosilicate glass and aluminum. As an example, Fig. 11 is an SEM photo of 0.65 μm thick polysilicon that was reactive ion etched using the tri-level structure initially patterned with x-ray lithography as a mask. There is seen to be very little (<0.1 μm) linewidth loss in the etched polysilicon.

III. CONCLUSION

The steep-profile three-layer pattern generation technique (tri-level) presents many potential advantages and applications to all phases of lithography. For optical lithography, it can allow preparation of fine feature devices using present optical exposure systems. For x-ray and electron lithography, submicron resolution features with better linewidth control and good step coverage are possible.

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